10/750250

CofC

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313 on 31 May 2006.

#35,589

Jeff Lloyd, Patent Attorney

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 CFR 1.322
Docket No. SUN-DA-135T
Patent No. 7,008,856

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Chang Hun Han
Issued	:	March 7, 2006
Patent No.	:	7,008,856
For	:	Method for Fabricating AND-Type Flash Memory Cell

Mail Stop Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE OF CORRECTION
UNDER 37 CFR 1.323 (APPLICANT MISTAKE)

Sir:

A Certificate of Correction (in duplicate) for the above-identified patent has been prepared and is attached hereto.

In the left-hand column below is the column and line number where error occurred in the patent. In the right-hand column is the page and line number in the application where the correct information should have appeared.

Patent Reads:	**Application Should Read:**
Column 1, line 34:	Page 1, lines 4 of [0004]:
"pattern 15"	--pattern 17--

06/06/2006 MGEBREM2 00000026 190065 7008856
01 FC:1811 100.00 DA

A true and correct copy of page 1 of the specification as filed accompanies this Certificate of Correction, showing the typographical error at line 4 of [0004] and the correct information at line 3 of [0005].

The Commissioner is authorized to charge the fee of $100.00 for the amendment to Deposit Account No. 19-0065. The Commissioner is also authorized to charge any additional fees as required under 37 CFR 1.20(a) to Deposit Account No. 19-0065. Two copies of this letter are enclosed for Deposit Account authorization.

Approval of the Certificate of Correction is respectfully requested.

Respectfully submitted,

Jeff Lloyd
Patent Attorney
Registration No. 35,589
Phone No.: 352-375-8100
Fax No.: 352-372-5800
Address: P.O. Box 142950
Gainesville, FL 32614-2950

JL/fes
Attachments: Copy of page 1 of the specification

2006

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,008,856

APPLICATION NO.: 10/750,250

DATED : December 31, 2003

INVENTORS : Chang Hun Han, Bong Kil Kim

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 1,
Line 34, "pattern 15" should read --pattern 17--.

MAILING ADDRESS OF SENDER:
Saliwanchik, Lloyd & Saliwanchik
P.O. Box 142950
Gainesville, FL 32614-2950

JUN 8 2006

METHOD FOR FABRICATING AND-TYPE FLASH MEMORY CELL

FIELD OF THE DISCLOSURE

[0001] The present disclosure relates generally to semiconductor devices and, more particularly, to a method for manufacturing an AND type flash memory device.

BACKGROUND

[0002] In fabricating a flash memory device, the cell array is an important factor determining a type of a flash memory device together with a memory device structure, an erasing method, and a programming method. Among various cell array structures, AND-type cell arrays can embody the density and the high-performance operation of a flash memory.

[0003] Fig. 1 is a schematic diagram illustrating a cell array of a conventional AND-type flash memory device. The conventional AND-type flash memory device embodies densification (i.e., greater density) by sharing bit line contacts and source lines in a plurality of cells and suppresses the occurrence of disturbances during program operation through parallel connection and the layered bit lines and source lines. However, a conventional AND-type flash memory device has a shortcoming in that interconnection density in a diffusion layer is high.

[0004] Figs. 2a through 2h illustrate, in cross-sectional views, the fabricating process of an AND-type flash memory device according to a conventional method. Referring to Fig. 2a, a pad oxide layer 13 and a pad nitride layer 15 are deposited in sequence on a silicon substrate 11. Then, a photoresist pattern 15 is formed on the pad nitride layer 15.

[0005] Referring to Fig. 2b, some part of the pad nitride layer 15, the pad oxide layer 13, and the substrate 11 is removed by an etching process using the photoresist pattern 17 as a mask. As a result, a pad oxide pattern 13a and a pad nitride pattern 15a